ABSTRACT OF THE DISCLOSURE

[1059] In a programmable memory array, multiple memory cells on a single bit line may be tested in parallel for the unprogrammed state by simultaneously selecting multiple word lines associated with a selected bit line within a sub-array. A read current flowing through each selected memory cell is added on the selected bit line, and may be sensed using the same bit line sense circuits used for normal read operations. In the test mode, the sense circuit preferably indicates a pass/fail condition for all N simultaneously selected memory cells, which may be directly conveyed as an output signal, or may be combined with other similar pass/fail signals from other selected bit line sense circuits to generate a combined pass/fail output signal. Multiple bit lines may be simultaneously selected within the same sub-array. In addition, multiple sub-arrays may be simultaneously selected, each having one or more simultaneously selected bit lines, and the respective pass/fail signals conveyed directly or combined into fewer numbers of such signals.